

## GENERAL DESCRIPTION

The Xelic 10Gb Ethernet Rate Adaptation Core (XCE10GA) performs rate adaptation through the insertion and removal of complete PCS blocks containing idle characters to provide maximum transparency capability. Optional Flow control is provided through the insertion of programmable PAUSE frames in open or closed loop configurations. 10GBASE-R and 10GBASE-W applications are supported with 64B/66B transmission codes transferred at a 10Gb rate using a 64-bit data bus operating at 161.13Mb/s.

The XCE10GA Transmit Processor accepts incoming 64B/66B codes and performs block synchronization with optional descrambling/scrambling capability. Programmable bypass, rate adaptation, and loopback modes of operation are supported. Rate adaptation is achieved through the removal of complete PCS block idles when enabled through external signal control. A BER monitor provides an indication of signal integrity for incoming data blocks. Test Block insertion is provided for diagnostic purposes in addition to configurable Error Block insertion for programmable LOS, high BER, and Loss of Block Lock (LOBL) error detection.

The XCE10GA Receive Processor contains a configurable block synchronizer with options for block scrambling/descrambling capability. Rate adaptation is achieved through the insertion of complete PCS block idles when enabled in rate adaptation mode. A BER monitor provides an indication of signal integrity for incoming data blocks. Error Blocks are optionally inserted for programmable LOS, high BER, and Loss of Block Lock (LOBL) error detection. Test Block compare capability with maskable interrupt error reporting capability is supported. Optional flow control is enabled through the insertion of programmable PAUSE frames by the receive processor. A programmable open or closed loop flow control mechanism is provided.

Performance counters are provided for the accumulation of Synchronization Block Error, BER Error and Block Idle conditions in the XCE10GA transmit processor. In addition, the receive processor contains Synchronization Block Error, BER Error and Test Block Mismatch performance counters. All counters are configurable for saturating latch and clear operation or periodic error sync auto-update mode.

The XCE10GA provides facility and terminal loopback modes of operation using Transmit and Receive Processor data path configurations for system debug purposes.

A 16-bit generic register interface for access and configuration of internal memory mapped locations is included.

## FEATURES

- Suitable for FPGA and/or ASIC implementations.
- Integration support and maintenance available.
- XCE10GA core available under flexible single use licensing terms with netlist or source code deliverables.
- Implements flexible data bus architecture.
- Provides bypass and rate adaptation modes of operation.
- Implements 16-bit register interface for programming of internal registers.
- Complies with IEEE802.3 specification.
- Supports transmit and receive facility and terminal loopback configurations.
- Performs rate adaptation through the removal of complete block idles.
- Provides transmit and receive PCS block synchronization with programmable Out Of Block Lock (OOBL) and Loss Of Block Lock (LOBL) detection and maskable interrupt capability.
- Supports transmit and receive incoming BER monitoring with optional interrupt reporting.
- Provides optional scrambling  $(1 + x^{39} + x^{58})$  with polynomial corruption capability for diagnostics.
- Supports programmable Test Block insertion for diagnostic purposes.
- Provides transmit processor programmable Error Blocks insertion for a variety of maskable error conditions including LOS, high BER detection, LOBL, and rate adaptation error detection.
- Performance Synchronization Block Error, BER Error and Block Idle counters are provided with user defined interval or errored second accumulation.
- Performs rate adaptation through the insertion of complete block idles.
- Supports open and closed loop flow control through the insertion of programmable PAUSE frames when PAUSE Frame insertion is enabled.
- Provides receive processor programmable Error Blocks insertion for a variety of maskable error conditions including receive LOS, high BER detection, and LOBL error detection.
- Supports programmable test block detection with interrupt reporting capability.

## APPLICATIONS

- OTN 10Gb/s Rate Adaptation
- DWDM and WDM systems
- SONET/SDH WIS Framer
- OTN and/or SONET/SDH line cards
- Test Equipment