

GENERAL DESCRIPTION

The Xelic Frame Mapped Generic Framing Procedure Core (XCGFPFM) will frame and encapsulate/de-encapsulate client traffic in compliance with ITU-T G.7041/Y.1303. GFP Transmit and Receive Processors function independently to provide full duplex operation at data rates up to 2.5Gb/s with a common register interface for core configuration and control. GFP processing in either direction can be throttled or suspended at any time by de-asserting transmit and/or receive enable inputs. This feature enables the XCGFPFM core to be used in systems with variable line data rates.

The GFP transmit processor accepts incoming frame mapped data packets (Ethernet, PPP, MAPOS, or proprietary packets) or management packets from an external FIFO interface and packages them into GFP client data frames. GFP control frames (idles) are inserted to achieve frame rate adaptation when incoming client packet information is not available. GFP payload information is optionally scrambled using a $x^{43} + 1$ self synchronous scrambling algorithm. A 4-byte GFP core header is added each frame and is optionally scrambled using a Barker like sequence. A test feature is provided to allow for the self generation of GFP frames and the corruption of core and/or payload header HEC fields.

The GFP receive processor performs frame delineation and optionally corrects core and payload header single bit errors (multiple bit errors are detected). Interpreters are implemented to detect control frames (idles), client management frames, client data frames, corrupted frames, and invalid client data and management frame conditions.

The XCGFPFM provides a generic register interface for access and configuration of internal memory mapped locations. This interface is shared between GFP transmit and receive processors with addressing being mapped from independent base addresses. The implementation of a generic register interface allows for easy integration with other cores that may be contained in a customer application.

FEATURES

- XCGFPFM core available under flexible single use or perpetual licensing terms with netlist or source code deliverables
- Suitable for FPGA and/or ASIC implementations
- Compliant with ITU-T G.7041/Y.1303 Specification
- Supports all frame mapped client data types (Ethernet, PPP, MAPOS, Propriety Packet)
- Allows transport of any client management frame type
- Operates at data rates up to 2.488Gb/s (OC-48)
- Provides optional core header (Barker-like sequence of length 32) and payload header (self synchronous $x^{43}+1$ polynomial) scrambling/ descrambling
- Provides generic register interface for programming of internal registers
- Test mode available for generation of user specified client data or client management frame types
- Optionally calculates and inserts FCS
- Provides 16-bit counters for the accumulation of GFP control frames generated, client data packets transmitted, and client management packets transmitted
- Supports pad character insertion for SOP error conditions
- Performs frame delineation on incoming GFP frames with optional cHEC descrambling
- Supports core and payload header single bit error correction (optional) and multiple bit error detection
- Provides detection and accumulation of SSF errors, FCS errors, core header corrected, payload header corrected, payload headed uncorrected, control frame, client management packet, client data packet, and client invalid packet conditions to provide an indication of health status for the incoming GFP data link

APPLICATIONS

- OTN/SONET add/drop multiplexers
- Optical and/or digital switch
- Digital cross connects
- OTN and/or SONET/SDH line cards
- Test equipment

OPTICAL SWITCH APPLICATION

