

**GENERAL DESCRIPTION**

The Xelic OTN 40Gb/s FEC Decoder (XCO3FECD) core detects and corrects incoming errors using interleaved Reed Solomon (255,239) codes for Optical Transport Network applications. Interleaving is performed as outlined in specification G.709 with FEC codewords containing 255 byte symbols made up of 239 byte data symbols and 16 byte check symbols. The XCO3FECD can be parameterized to support 128 or 256 bit data widths.

The XCO3FECD accepts incoming data for interleaving and FEC decoding. Interleaving is performed by dividing 3824 bytes from each row of the ODUk frame structure into 16 sub-rows prior to FEC decoding. The XCO3FECD contains *m* independent instances of Reed Solomon (255,239) decoders, where *m* is the data bus width size option of the core chosen in bytes to decode the sixteen byte-interleaved sub-rows of data. Interleaved frames are interpreted with correctable and uncorrectable errors identified and accumulated in dedicated counters. The decoder algorithm implemented allows for correction of up to sixteen errors per codeword or 512 erroneous bytes per frame. If more than sixteen errors are detected, the codeword is marked as invalid. A de-interleaving stage follows FEC decoding to organize outgoing data into the proper format while performance counters are being updated.

An integrated FEC Signal Degrade block accumulates bit-errors over a fixed frame-based time interval and compares it to one of two configurable

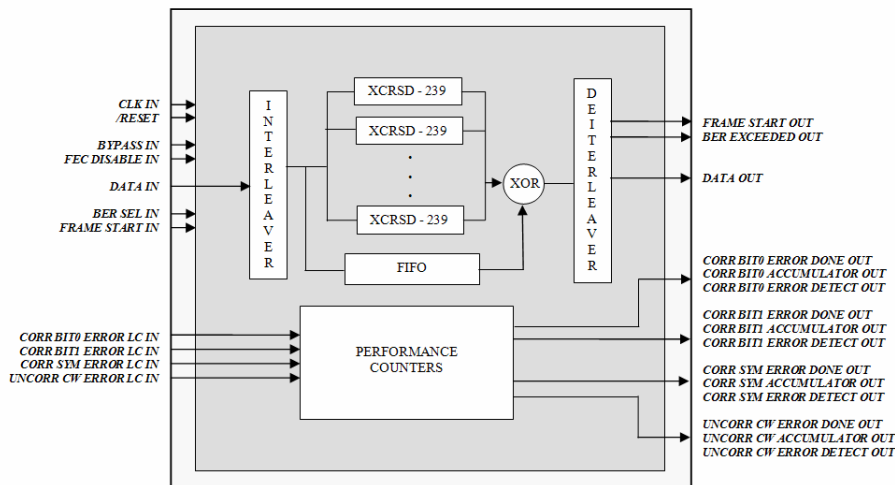
threshold constants. The XCO3FECD core supports normal, sleep, and bypass modes of operation. Saturating performance counters are provided for the accumulation of correctable symbols, correctable 0's, correctable 1's, and uncorrectable codewords.

**FEATURES**

- Suitable for FPGA and/or ASIC implementations.
- Integration support and maintenance available.
- The XCO3FECD core is available under flexible single use licensing terms with netlist or source code deliverables.
- Implements flexible data bus architecture.
- Provides for normal and bypass modes of operation.
- Complies with ITU-T G.709 and ITU-T G.798 specifications.
- Corrects up to sixteen errors per codeword or 512 erroneous bytes per frame.
- Supports normal, sleep, and bypass modes of operation.
- Provides performance counters for the accumulation of FEC correctable symbols, correctable 0's, correctable 1's, and uncorrectable codewords.
- Supports configurable FEC bit error rate detection of  $10^{-3}$  or  $10^{-4}$ .

**APPLICATIONS**

- OTN Framer
- OTN and/or SONET/SDH line cards
- Test Equipment



**XCO3FECD Block Diagram**