

**GENERAL DESCRIPTION**

The Xelic OTN 40Gb/s FEC Encoder (XCO3FECE) core generates interleaved Reed Solomon (255,239) codes for Optical Transport Network applications. Interleaving is performed as outlined in specification G.709 with FEC codewords containing 255 byte symbols made up of 239 byte data symbols and 16 byte check symbols. The XCO3FECE can be parameterized to support 128, or 256 bit data widths.

The XCO3FECE accepts incoming data for interleaving and FEC coding when the associated data enable input is asserted. The calculated parity check bytes are generated and provided at the core outputs when the data enable input is deasserted. Interleaving is performed by dividing 3824 bytes from each row of the ODUk frame structure into 16 sub-rows prior to FEC encoding. The XCO3FECE contains *m* independent instances of Reed Solomon (255,239) encoders, where *m* is the data bus width size option of the core chosen in bytes to encode the sixteen byte-interleaved sub-rows of data. A de-interleaving stage follows FEC encoding to organize

outgoing data into the same format as the original incoming data.

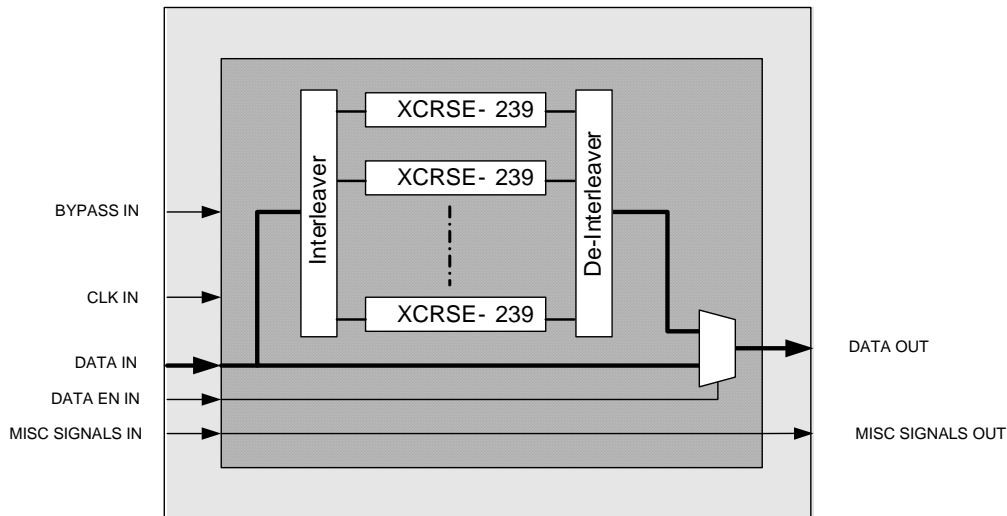
The XCO3FECE core supports normal and bypass modes of operation with optional miscellaneous signal synchronization capability.

**FEATURES**

- Suitable for FPGA and/or ASIC implementations.
- Integration support and maintenance available.
- The XCO3FECE core is available under flexible single use licensing terms with netlist or source code deliverables.
- Implements flexible data bus architecture.
- Provides for normal and bypass modes of operation.
- Complies with ITU-T G.709 and ITU-T G.798 specifications.

**APPLICATIONS**

- OTN Framer
- OTN and/or SONET/SDH line cards
- Test Equipment



**XCO3FECE Block Diagram**