

GENERAL DESCRIPTION

The Xelic SONET/SDH Concatenated STS-12c/STM-4 Framer Core (XCS12C) aligns incoming SONET/SDH frames and provides transport overhead processing, path overhead processing and pointer processing for contiguous concatenated SONET/SDH payloads types. The XCS12C contains independent Transport Processor and Concatenated Path Processor modules with dedicated external ports for overhead insertion and extraction. Incoming/outgoing data is transferred at an STS-12c/STM-4 rate using an 8-bit data bus operating at 77.76Mb/s.

The XCS12C Transmit Transport Processor inserts transport overhead, calculates and inserts B1/B2 parity (with corruption capability), automatically generates line RDI, and scrambles (with corruption capability) SONET/SDH frames. A programmable trace buffer is implemented for 1 byte, 16 byte or 64 byte trace message insertion. Diagnostics support includes optional corruption of inserted parity, corruption of scrambling, framing corruption, and programmable generation of line AIS, and line RDI conditions.

The XCS12C Transmit Concatenated Path Processor inserts high order path overhead, calculates and inserts B3 parity (with corruption capability), and automatically generates path RDI. A programmable trace buffer is implemented for 16 byte or 64 byte trace message insertion. Normal and bypass modes of operation are supported. In normal mode, incoming payload information is requested for insertion into the outgoing SONET/SDH SPE frame cavity. A fixed outgoing pointer is provided with an option to program any legal value (0 to 782) for generated frames. POH byte information can be inserted through internal register control or from an external overhead port.

The XCS12C Receive Transport Processor contains a configurable frame alignment unit with programmable options for OOF and LOF algorithm state transitions. Incoming frames are descrambled (optional) and aligned for transport overhead processing. Transport overhead information is extracted to internal register locations and dedicated section DCC, line DCC, section orderwire, line orderwire, and transport overhead external ports. Transport overhead interpreters are implemented to detect and report various error conditions which include LOS, LOF, LOA, OOF, B1, SD, SF, B2, AIS-L, and RDI-L with optional maskable interrupt generation provided. LOS detection is available through an incoming signal or an internal programmable LOS detection algorithm. Section Trace messages of 16 or 64 byte lengths are evaluated for trace identifier mismatch (TIM-L) and trace identifier unstable (TIU-L) conditions. Line AIS is inserted through programmable internal register control. Diagnostics support includes optional corruption of calculated parity, corruption of descrambling, and Line AIS generation.

The XCS12CPP Receive Concatenated Path Processor extracts high order path overhead to both internal registers and an external path overhead port. Path Trace messages

of 16 or 64 byte lengths are evaluated for trace identifier mismatch (TIM) and trace identifier unstable (TIU) conditions. Path AIS is optionally inserted and maskable interrupts are generated for detected Path Trace Identifier Unstable (TIU-P), Path Trace Identifier Mismatch (TIM-P), Signal Degrade (SD), Signal Fail (SF), Path Signal Label Unstable, and/or Path Unequipped (UNEQ-P) error conditions. An incoming path RDI interpreter reports detected RDI-P, ERDI-P, and path RDI unstable errors. Incoming Synchronous Payload Envelope (SPE) information is extracted and passed to the external system side interface with valid data indication provided through a dedicated output.

Performance counters (configurable for bit or block count type) are provided for the accumulation of detected OOF, B1 parity, B2 parity B3 parity, REI-L errors, REI-P errors, pointer increment or decrement events, and pointer NDF occurrences for incoming SONET/SDH frames. B2 and B3 parity errors are accumulated with programmable threshold capability for signal degrade (SD) and signal fail (SF) detection. Counters are configurable for saturating latch and clear operation or periodic error sync auto-update mode.

The XCS12C provides a variety of facility and terminal loopback modes of operation for Transport Processor and Concatenated Path Processor functions using Transmit and Receive Processor data path configurations for system debug purposes.

A 16-bit generic register interface for access and configuration of internal memory mapped locations is included.

FEATURES

- Suitable for FPGA and/or ASIC implementations.
- Integration support and maintenance available.
- XCS12C core available under flexible single use licensing terms with netlist or source code deliverables.
- Implements flexible data bus architecture.
- Provides for bypass and normal modes of operation.
- Implements 16-bit register interface for programming of internal registers.
- Compliant with ITU-T G.707 and Telcordia GR-253-CORE Specifications.
- Inserts transport and high order path overhead through internal register programming and/or external overhead ports.
- Provides transmit facility and terminal loopback options for diagnostic purposes.
- Supports transport overhead insertion through dedicated external section DCC, line DCC, section orderwire, line orderwire, and transport overhead ports.
- Provides automatic REI-L insertion for B2 parity errors detected in the XCS12C Receive Processor.
- Allows for the insertion of programmable 1, 16 or 64 byte trace messages.
- Calculates and inserts B1/B2/B3 parity information with optional corruption capability.

- Allows for programmable automatic insertion of line RDI for the detection (Receive Transport Processor) of Loss of Signal (LOS), Loss of Frame (LOF), Loss of Alignment (LOA), Out of Frame (OOF), Alarm Indication Signal (AIS-L), Remote Defect Indication (RDI-L), Signal Fail (SF), Signal Degrade (SD), Trace Identifier Mismatch (TIM-L), or Trace Identifier Unstable (TIU-L) conditions.
- Provides extended programmable diagnostics capability to force line AIS-L, LOS, RDI-L, and frame corruption insertion.
- Provides automatic path REI insertion (bit or block mode options) for B3 parity errors detected in the XCS12CPP Receive Processor.
- Allows for programmable automatic insertion of single bit or enhanced path RDI for the detection (XCS12CPP Receive Processor) of Path Alarm Indication Signal (AIS-P), Loss of Pointer (LOP-P), Path Trace Identifier Mismatch (TIM-P), Path Trace Identifier Unstable (TIU-P), Path Unequipped (UNEQ-P), and Path Signal Label Mismatch (PLM-P) conditions.
- Supports programmable fixed payload data insertion for diagnostic purposes.
- Provides flexible frame alignment capability with programmable options for OOF and LOF algorithm state transitions. Diagnostic capability is provided to force LOF and OOF state conditions.
- Extracts transport and high order path overhead to internal register locations and dedicated external ports for section DCC, line DCC, section orderwire, line orderwire, and transport overhead.
- Supports optional SONET/SDH frame scrambling/descrambling with programmable descrambler corruption capability for diagnostic purposes.
- Supports the programmable insertion of Line AIS frames. Diagnostic capability is provided to force a line AIS condition.
- Provides independent 16-bit saturating performance counters with programmable latch and clear or incoming error sync capture options.
- Provides section and path trace interpreter with programmable trace accept and unstable counts for message lengths of 1, 16 or 64 bytes. Optional maskable interrupt generation is provided for Line/Path Trace Identifier Mismatch (TIM-L, TIM-P) and Line/Path Trace Identifier Unstable (TIM-L, TIM-P) error detection.
- Provides LOS detection through a selectable dedicated external input or programmable internal LOS state machine.
- Interprets and extracts F1, APS, S1 (optional byte or nibble detection) overhead information to internal register locations with programmable accept and inconsistent maskable interrupt capability.
- Detects LOS, LOF, LOA, OOF, TIM, TIU, B1 error, SD, SF, B2 error, AIS-L, and RDI-L conditions and provides optional interrupt generation.
- Provides pointer interpreter functionality with programmable state machine operation including the 8 of 10 pointer objective and single AIS state transition options for flexible configurations.
- Detects and accumulates pointer interpreter increments, decrements, and NDF events.
- Provides programmable automatic insertion of Path Alarm Indication Signal (AIS-P) for the detection of Path Trace Identifier Unstable (TIU-P), Path Trace Identifier Mismatch (TIM-P), Signal Degrade (SD), Signal Fail (SF), Path Signal Label Unstable, and Path Unequipped (UNEQ-P).
- Interprets and extracts F2, F3, and K3 (optional byte or nibble detection) path overhead information to internal register locations with programmable accept and unstable maskable interrupt capability.
- Interprets incoming path RDI overhead information (provides programmable accept and unstable counts) and provides detection of RDI-P, ERDI-P, and path RDI unstable errors with maskable interrupt capability.

APPLICATIONS

- OTN/SONET add/drop multiplexers
- SONET/SDH switch
- Digital cross connects
- OTN and/or SONET/SDH line cards
- Test equipment