

GENERAL DESCRIPTION

The Xelic SONET/SDH Tributary Payload Processor Core (XCS3TPP) performs tributary pointer processing, aligns outgoing tributaries and provides tributary path overhead error detection and performance monitoring. The XCS3TPP implements the industry standard telecom bus architecture for interfacing of various signaling and data transfers with support for incoming parity checking and outgoing parity generation to ensure data integrity. Incoming/outgoing data is transferred at an STS-3/STM-1 rate using an 8-bit data bus operating at 19.44Mb/s.

SONET and SDH modes of operation are supported with flexible configurations and monitoring options available for control and visibility of individual tributaries. SONET mode provides the capability for processing STS-3 streams containing any legal mix of VT1.5, VT2, VT3, or VT6 tributaries. SONET tributary information is contained within virtual tributary groups (VT Group) of STS-1 or STS-3 level frame structures. Each VT group can be configured for 4xVT1.5, 3xVT2, 2xVT3, or 1xVT6. SDH mode provides processing for any legal mix of TU11, TU12, TU2 or TU3 tributaries. SDH STM-1 frames contain AU-3 or AU-4 structures that transport combinations of TUG-2 or TUG-3 frame structures. TUG-3's can be configured to contain seven TUG2's or a single TU3 tributary. TUG2's can be configured for 4xTU11, 3xTU12, 2xSDH VT3 equivalent, or 1xTU2.

Configurable incoming multi-frame information is detected and analyzed to provide pointer locations for each tributary processed. Tributary pointer processing provides detection for loss of pointer (LOP-V/TU-LOP) and alarm indication signal (AIS-V/TU-AIS) conditions with optional interrupt capability available. Additionally, pointer justification (increment/decrement) events are tracked and reported.

Tributary payload processing supports the interpretation of path overhead bytes and provides detection of REI-V/LP-REI, RFI-V/LP-RFI, UNEQ, Path Signal Label accepted and inconsistent, Path Trace accepted and inconsistent and RDI-V/LP-RDI conditions with optional interrupt capability. Path trace message lengths of 16 and 64 byte lengths are supported for all tributaries through internal register configuration.

Performance counters (configurable for bit or block count type) are provided for the accumulation of BIP-2/BIP-8 (TU-3) and REI-V/LP-REI errors for each tributary with BIP-2/BIP-8 programmable threshold capability for signal degrade (SD) and signal fail (SF) detection. Counters are configurable for saturating latch and clear operation or periodic error sync auto-update mode.

The XCS3TPP provides outgoing tributary pointer generation and alignment with multi-frame synchronization available from an external input or through automatic internal generation. An external tributary synchronization is also provided through CIJ1V1 and SPE valid signaling. Transport (optional) and path (except H4) overhead

blanking is provided for outgoing SONET/SDH frames (except STS-1's in bypass mode).

A 16-bit generic register interface for access and configuration of internal memory mapped locations is included.

FEATURES

- Suitable for FPGA and/or ASIC implementations
- Supports industry standard Telecom Bus interface
- Implements 8-bit data bus architecture
- Supports Tributary Payload Processing for SONET (STS-3) and SDH (STM-1) modes of operation.
- SONET mode processing provided for any legal mix of VT1.5, VT2, VT3, or VT6 tributaries. Each VT group can be configured for 4xVT1.5, 3xVT2, 2xVT3, or 1xVT6.
- SDH mode processing provided for any legal mix of TU11, TU12, TU2 or TU3 tributaries. Each TUG2 can be configured for 4xTU11, 3xTU12, or 1xTU2. A TUG3 can be configured to contain seven TUG2's or a single TU3 tributary.
- Inserts an all 0's byte pattern for TOH (optional) and POH (except H4) overhead byte locations or allows pass thru of incoming values in STS-1 bypass mode.
- Configurable multi-frame detection of incoming channels through either MF signaling (optional H4 byte detection/V1 byte position) or interpretation of H4 (utilizes IC1J1V1/ISPE inputs).
- Inserts internally generated multi-frame information into H4 byte with leading logic 1's for outgoing data channels.
- Aligns outgoing VT/TU's through insertion of selectable outgoing pointer values of 0 or 522 for SONET/SDH STS-3/STM-1 frames.
- Optional masking of tributary overhead interpreter and payload processing function interrupt condition reporting.
- Calculates and compares V5/B3 BIP-2/ BIP-8 (TU3) parity for all incoming tributaries.
- Detects RFI-V/LP-RFI and RDI-V/LP-RDI for all incoming tributaries and provides interrupt capability.
- Provides 16-bit saturating counters (configurable for bit or block type) for the accumulation of BIP-2/BIP-8 and REI-V/LP-REI errors with individual programmable threshold (BIP-2/BIP-8) capability (including optional error sync update capability) for each tributary. Provides optional interrupt generation for signal degrade (SD) and signal fail (SF) detection.
- Detects LOP-V/TU-LOP, AIS-V/TU-AIS, and UNEQ-V/LP-UNEQ conditions for all tributaries and provides optional interrupt generation.
- Provides insertion of tributary AIS-V/TU-AIS or UNEQ-V/LP-UNEQ conditions through optional internal control.
- Detects Loss of Multi-frame (LOM) and generates optional interrupts for each incoming tributary.
- Calculates and compares incoming Telecom Bus parity (odd or even type with selectable *CIJ1V1 IN* and/or

- *SPE IN* input signal inclusion for calculation) with optional interrupt generation on errors.
- Generates outgoing odd or even Telecom Bus parity with selectable *CIJIVI IN* and/or *SPE IN* input signal inclusion for calculation.
- Generates output signaling for identification of STM-1/STS-3 Start of Frame (SOF) and Tributary Multi-Frame (TMF) positions.
- Provides outputs for identifying individual tributary SPE, V5/J1 indicators, LOM, LOP-V/TU-LOP, AIS-V/TU-AIS, and UNEQ-V/LP-UNEQ conditions.
- Supports outgoing tributary alignment for internally or externally generated multi-frame sync signaling enabled through internal register programming.
- Processes incoming tributary path signal label overhead information and detects tributary path signal label accepted and unstable conditions in addition to providing optional interrupt generation.
- Extracts all incoming J2 (J1 byte for TU-3) tributary trace path messages to a configurable 16 or 64 byte trace buffer with trace identifier accepted and unstable detection (includes optional interrupt generation).

- Provides 16-bit register interface for programming of internal registers
- XCSTPP core available under flexible single use or perpetual licensing terms with netlist or source code deliverables.
- Integration support and maintenance available.

APPLICATIONS

- OTN/SONET add/drop multiplexers
- SONET/SDH switch
- Digital cross connects
- OTN and/or SONET/SDH line cards
- Test equipment