

## GENERAL DESCRIPTION

The Xelic SONET/SDH Concatenated Framing Core (XCS48CN) aligns incoming SONET/SDH frames and provides transport overhead processing, path overhead processing and pointer processing for contiguous concatenated SONET/SDH payloads types. The XCS48CN contains independent Transport Processor and Concatenated Path Processor modules for STS-48/STM-16 SONET/SDH frame rates. Incoming/outgoing data is transferred at clock rate of 155.52 MHz using a 16-bit data bus.

The XCS48CN Transmit Transport Processor inserts transport overhead blanking, calculates and inserts framing, B1/B2 parity (with corruption capability), and scrambles SONET/SDH frames. Diagnostics support includes optional corruption of inserted parity, and scrambling enable/disable capability. MS AIS insertion is also provided.

The XCS48CN Transmit Concatenated Path Processor inserts high order path overhead blanking, calculates and inserts B3 parity (with corruption capability), and supports pointer increment and decrements. AISP insertion is also provided.

The XCS48CN Receive Transport Processor contains a frame alignment unit with OOF and LOF algorithm state transitions. Incoming frames are descrambled (optional) and aligned for transport overhead processing. Transport overhead interpreters are implemented to detect error conditions which include LOS, LOF, OOF, B1 errors, B2 errors, and MS AIS. Diagnostics support includes optional corruption of calculated parity, and descrambling enable/disable capability.

The XCS48CN Receive Concatenated Path Processor detects Path AIS, LOP, Pointer Increments, Pointer Decrements, Pointer NDF's, POINTER 3 in a row conditions, and B3 error detection.

## FEATURES

- Suitable for FPGA and/or ASIC implementations.
- Integration support and maintenance available.
- The XCS48CN core is available under flexible single use licensing terms with netlist or source code deliverables.
- Compliant with ITU-T G.707 and Telcordia GR-253-CORE Specifications.
- Supports transport and path overhead blanking.
- Supports optional SONET/SDH frame scrambling for diagnostic purposes.
- Calculates and inserts B1/B2/B3 parity information with optional corruption capability.
- Provides capability to force MS AIS, path AIS, or LOS insertion.
- Provides ability to force pointer increment and decrement operations.
- Supports incoming frame alignment with OOF and LOF algorithm state transition signaling.
- Supports optional SONET/SDH frame descrambling for diagnostic purposes.
- Detects LOS, LOF, OOF, B1 error, B2 error, B3 error, Path AIS, and MS AIS conditions.
- Calculates and compares extracted B1/B2/B3 parity for all incoming SONET/SDH frames.
- Detects LOP, pointer interpreter increments, decrements, pointer NDF, and pointer 3 in a row events.

## APPLICATIONS

- OTN/SONET add/drop multiplexers
- SONET/SDH switch
- Digital cross connects
- SONET/SDH line cards
- Test equipment