

GENERAL DESCRIPTION

The Xelic SONET/SDH Channelized High Order Path Processor Core (XCS48PP) performs path overhead processing and pointer processing for any mix of SONET/SDH payloads ranging from a granularity of STS-1 to STS-48c including non-standard concatenation types. The XCS48PP contains independent transmit and receive processors with dedicated external path overhead ports and a generic register interface to provide flexible insertion and extraction capability. Incoming/outgoing data is transferred at an STS-48/STM-16 rate using a 32-bit data bus operating at 77.76Mb/s.

The XCS48PP Transmit Processor inserts channelized path overhead, calculates and inserts B3 parity (with corruption capability), automatically generates path RDI, and supports Tandem Connection source or sink configurations with programmable Incoming Signal Fail (TC-ISF) detection. A programmable trace buffer is implemented for 16 byte or 64 byte trace message insertion. An integrated pointer interpreter provides programmable state machine operation which includes options for 8 of 10 pointer objective and single AIS state transitions. Incoming Synchronous Payload Envelope (SPE) information is extracted for each path and passed through an internal FIFO for insertion into outgoing SONET/SDH frames. A pointer generator is provided for applications with different clocks (nearly same timing) at the line and system side interfaces (plesiochronous boundaries). Diagnostics support includes fixed payload data insertion down to an STS-1 granularity, AIS-P or VC-AIS generation, and the ability to manipulate pointers (pointer increment, decrement, NDF capability) in outgoing SONET/SDH frames. A flexible system side interface is provided for synchronized frame start or telecom bus signaling.

The XCS48PP Receive Processor extracts channelized path overhead to both internal registers and an external path overhead port. Path Trace messages of 16 or 64 byte lengths are evaluated for trace identifier mismatch (TIM) and trace identifier unstable (TIU) conditions. Tandem Connection source or sink configurations with programmable Incoming Signal Fail (TC-ISF) detection is provided. Path AIS is optionally inserted and maskable interrupts are generated for detected Path Trace Identifier Unstable (TIU-P), Path Trace Identifier Mismatch (TIM-P), Signal Degrade (SD), Signal Fail (SF), Path Signal Label Unstable, Path Unequipped (UNEQ-P), and/or Loss of Multiframe (LOM) error conditions. An incoming path RDI interpreter reports detected RDI-P, ERDI-P, and path RDI unstable errors. Incoming Synchronous Payload Envelope (SPE) information is extracted for each path and passed through an internal FIFO for insertion into outgoing SONET/SDH frames. A pointer generator is provided for applications with different clocks (nearly same timing) at the line and system side interfaces (plesiochronous boundaries). Diagnostics support includes fixed payload data insertion down to an STS-1 granularity, AIS-P or VC-AIS generation, and the ability to manipulate pointers (pointer increment, decrement, NDF capability) in outgoing

SONET/SDH frames. Synchronous frame start and telecom bus signaling is generated at the system side interface to identify various SONET/SDH frame byte positions.

Performance counters (configurable for bit or block count type) are provided for the accumulation of detected Tandem Connection IEC errors, B3 parity errors, Path REI errors, pointer increment or decrement events, and pointer NDF occurrences for interpreted or generated pointer processing of SONET/SDH frames. B3 parity errors are accumulated with programmable threshold capability for signal degrade (SD) and signal fail (SF) detection. Counters are configurable for saturating latch and clear operation or periodic error sync auto-update mode.

The XCS48PP provides facility and terminal loopback modes of operation for Transmit and Receive Processor data path configurations for system debug purposes.

A 16-bit generic register interface for access and configuration of internal memory mapped locations is included.

FEATURES

- Suitable for FPGA and/or ASIC implementations.
- Integration support and maintenance available.
- XCS48PP core available under flexible single use licensing terms with netlist or source code deliverables.
- Supports bypass, loopback, and normal modes of operation.
- Implements 16-bit register interface for programming of internal registers.
- Compliant with ITU-T G.707 and Telcordia GR-253-CORE Specifications.
- Supports processing for any mix of payloads ranging from a granularity of STS-1 to STS-48c including non-standard concatenation types.
- Provides transmit/receive facility and terminal loopback options for diagnostic purposes.
- Provides transmit and receive pointer interpreter/generation functionality with programmable state machine operation including the 8 of 10 pointer objective and single AIS state transition options for flexible configurations.
- Detects and accumulates pointer interpreter or pointer generator increments, decrements, and NDF events.
- Inserts/extracts channelized high order path overhead through internal register programming and/or an external overhead port.
- Supports auto generated or synchronized frame start (telecom bus or frame start signaling) generation.
- Allows for blanking of all high order path overhead (except H4) locations.
- Provides automatic path REI insertion (bit or block mode options) for B3 parity errors detected in the XCS48PP Receive Processor.
- Allows for the insertion of programmable 1, 16 or 64 byte trace messages.
- Calculates and inserts B3 parity information with optional corruption capability.

- Supports transmit/receive Tandem Connection source or sink configurations with programmable Incoming Signal Fail (ISF) detection and maskable interrupt reporting.
- Allows for programmable automatic insertion of single bit or enhanced path RDI for the detection (Receive Processor) of Path Alarm Indication Signal (AIS-P), Loss of Pointer (LOP-P), Path Trace Identifier Mismatch (TIM-P), Path Trace Identifier Unstable (TIU-P), Path Unequipped (UNEQ-P), and Path Signal Label Mismatch (PLM-P) conditions.
- Interprets transmit and receive incoming multiframe information and supports optional AIS-P insertion for programmable LOM detection with maskable interrupt reporting.
- Supports programmable fixed payload data insertion down to STS-1 granularity for diagnostic purposes.
- Provides programmable diagnostics capability to force AIS-P, VC-AIS, RDI-P, and pointer generator increment, decrement, or NDF conditions.
- Detects AIS-P, LOP-P, FIFO overflow and underflows, SS bit mismatch, TC-REI, and telecom bus parity errors with maskable interrupt reporting.
- Includes 16-bit saturating performance counters (configurable for bit or block type) for the accumulation of B3 errors with programmable threshold capability (including optional error sync update option). Provides optional interrupt generation for B3 error, signal degrade (SD) and signal fail (SF) detection.
- Includes 16-bit saturating performance counters (configurable for bit or block type) for the accumulation of REI-P errors with programmable latch and clear or incoming error sync capture options. Optional maskable interrupt generation is provided for REI-P error detection.
- Provides programmable automatic insertion of Path Alarm Indication Signal (AIS-P) for the detection of Path Trace Identifier Unstable (TIU-P), Path Trace Identifier Mismatch (TIM-P), Signal Degrade (SD), Signal Fail (SF), Path Signal Label Unstable, Path Unequipped (UNEQ-P), and Loss of Multiframe (LOM).
- Provides path trace interpreter with programmable trace accept and unstable counts for message lengths of 1, 16 or 64 bytes. Optional maskable interrupt generation is provided for Path Trace Identifier Mismatch (TIM-P) and Path Trace Identifier Unstable (TIM-P) error detection.
- Interprets and extracts F2, F3, and K3 (optional byte or nibble detection) path overhead information to internal register locations with programmable accept and unstable maskable interrupt capability.
- Interprets incoming path RDI overhead information (provides programmable accept and unstable counts) and provides detection of RDI-P, ERDI-P, and path RDI unstable errors with maskable interrupt capability.

APPLICATIONS

- OTN/SONET add/drop multiplexers
- SONET/SDH switch
- Digital cross connects
- OTN and/or SONET/SDH line cards
- Test equipment

SONET/SDH Channelized Switch Application

The SONET/SDH channelized switch application shown below is used to route channel payload data to/from various locations in a system. A series of line cards are plugged into a telecom bus backplane where channel information is routed through the use of a Channel Switch. The OC-48 line card contains cores for SONET/SDH Transport Processing (XCS48F) and channelized (STS-1 level) Path Processing (XCS48PP) providing full duplex capability at a data rate of 2.488Gb/s.

