

GENERAL DESCRIPTION

The Xelic SONET/SDH High Order VCAT/LCAS Mapper Core (XCS48VM) provides path overhead processing and pointer processing for any mix of SONET/SDH payloads ranging from a granularity of STS-1 to STS-48c and performs high order (STS-1/VC-3-Xv or STS-3c/VC-4-Xc) virtual concatenation (VCAT) with link capacity adjustment scheme (LCAS) support enabling hitless dynamic bandwidth reprovisioning. The XCS48VM allows up to 48 individual channelized STS-1/VC-3's or 16 STS-3c/VC-4 contiguous concatenated payloads to be virtually concatenated into configurable groups (VCG's) to provide flexible bandwidth allocation. The core contains independent transmit and receive processors with dedicated external path overhead ports and a generic register interface to provide flexible insertion and extraction capability. Incoming/outgoing data is transferred at an STS-48/STM-16 rate using a 32-bit data bus operating at 77.76Mb/s.

The XCS48VM Transmit Processor inserts path overhead, calculates and inserts B3 parity (with corruption capability), automatically generates path RDI, and provides bit or block mode path REI insertion. A programmable trace buffer is implemented for 16 byte or 64 byte trace message insertion. In VCAT/LCAS mode, high order path overhead H4 information is inserted to add, delete and control the capacity of SONET/SDH virtual concatenation groups for outgoing frames. Programmable Multiframe insertion (MF1 and MF2) common to all VCG's is provided with corruption capability for path debug purposes. Programmable Group ID (GID) and Sequence field (SQ) information identifies each member of a VCG. H4 control field (CNTRL) insertion is provided to synchronize the sink with the source through a sequence of specified command codes. An integrated CRC encoder is used to calculate a checksum which is inserted (with optional corruption) into the CRC-n location of the multiframe for each SONET/SDH frame to validate the integrity of control packets generated. A flexible line side interface is provided for synchronized or automatically generated frame start signaling.

The XCS48VM Receive Processor extracts channelized path overhead to both internal registers and an external path overhead port. Path Trace messages of 16 or 64 byte lengths are evaluated for trace identifier mismatch (TIM) and trace identifier unstable (TIU) conditions. Path AIS is optionally inserted and maskable interrupts are generated for detected Path Trace Identifier Unstable (TIU-P), Path Trace Identifier Mismatch (TIM-P), Signal Degrade (SD), Signal Fail (SF), Path Signal Label Unstable, Path Unequipped (UNEQ-P), and/or Loss of Multiframe (LOM) error conditions. An incoming path RDI interpreter reports detected RDI-P, ERDI-P, and path RDI unstable errors. Incoming Synchronous Payload Envelope (SPE) information is extracted for each path and passed to the system side interface. High order POH H4 interpretation provides VCAT mode multiframe detection (MF1 and MF2), CRC decode, and member status (MST - indicates status for each member of a VCG) with error detection

reporting. Interpretation of incoming Re-Sequence Acknowledge overhead (RS-ACK) is performed with appropriate indication passed to the XCS48VM Transmit Processor for the re-sequencing of members in a VCG due to add or drop commands issued. Internal memory provides for 125us of differential delay compensation introduced between member paths in a VCG without external memory requirements. An optional external memory interface allows for compensation of up to 256ms of differential delay.

Performance counters (configurable for bit or block count type) are provided for the accumulation of detected B3 parity errors, Path REI errors, pointer increment or decrement events, and pointer NDF occurrences for interpreted pointer processing of SONET/SDH frames. B3 parity errors are accumulated with programmable threshold capability for signal degrade (SD) and signal fail (SF) detection. Counters are configurable for saturating latch and clear operation or periodic error sync auto-update mode.

The XCS48VM provides facility and terminal loopback modes of operation using Transmit and Receive Processor data path configurations for system debug purposes.

A 16-bit generic register interface for access and configuration of internal memory mapped locations is included.

FEATURES

- Suitable for FPGA and/or ASIC implementations.
- Integration support and maintenance available.
- XCSF core available under flexible single use licensing terms with netlist or source code deliverables.
- Supports Link Capacity Adjustment Scheme (LCAS) to provide for "right size" data transport optimization through High Order VCAT with granularity down to the STS-1 (VC-3) level.
- Provides hitless data add and remove capability.
- Provides processing for any mix of payloads ranging from a granularity of STS-1 to STS-48c including STS-1/VC-3-Xv or STS-3c/VC-4-Xc signals.
- Internal memory provides for 125us of differential delay compensation introduced between member paths in a VCG without external memory requirements.
- Provides an optional external memory interface for compensation of up to 256ms of differential delay.
- Inserts and interprets POH VCAT/LCAS H4 byte information.
- Provides corruption of H4 byte stage 1 (MF1) and stage 2 (MF2) multiframe information for diagnostic purposes.
- Provides transmit facility and terminal loopback options for diagnostic purposes.
- Implements 16-bit register interface for programming of internal registers.
- Compliant with ITU-T G.7042, G.7043, GR-253-CORE, and G.707 Specifications.