

## GENERAL DESCRIPTION

The Xelic SONET/SDH Transport Processor Core (XCS768F) performs transport overhead processing, aligns incoming SONET/SDH frames and provides overhead interpretation with error detection and performance monitoring. The XCS768F contains independent transmit and receive processors with dedicated external ports for overhead insertion and extraction. Incoming/outgoing data is transferred at an STS-768/STM-256 rate using a 256-bit data bus operating at 155.52Mb/s.

The XCS768F Transmit Processor inserts transport overhead, calculates and inserts B1/B2 parity (with corruption capability), automatically generates line RDI, and scrambles (with corruption capability) SONET/SDH frames. A programmable trace buffer is implemented for 1 byte, 16 byte or 64 byte trace message insertion. Diagnostics support includes optional corruption of inserted parity, corruption of scrambling, framing corruption, and programmable generation of line AIS, and line RDI conditions.

The XCS768F Receive Processor contains a configurable frame alignment unit with programmable options for OOF and LOF algorithm state transitions. Incoming frames are descrambled (optional) and aligned for transport overhead processing. Transport overhead information is extracted to internal register locations and dedicated section DCC, line DCC, section orderwire, line orderwire, and transport overhead external ports. Transport overhead interpreters are implemented to detect and report various conditions which include LOS, LOF, LOA, OOF, B1 error, SD, SF, B2 error, AIS-L, and RDI-L errors with optional maskable interrupt generation provided. LOS detection is available through either an incoming signal or an internal programmable LOS detection algorithm. Section Trace messages of 16 or 64 byte lengths are evaluated for trace identifier mismatch (TIM) and trace identifier unstable (TIU) conditions. Line AIS is inserted through programmable internal register control. Diagnostics support includes optional corruption of calculated parity, corruption of descrambling, and Line AIS generation.

Performance counters (configurable for bit or block count type) are provided for the accumulation of detected OOF, B1 parity, B2 parity and REI errors for incoming SONET/SDH frames. B2 parity errors are accumulated with programmable threshold capability for signal degrade (SD) and signal fail (SF) detection. Counters are configurable for saturating latch and clear operation or periodic error sync auto-update mode.

The XCS768F provides facility and terminal loopback modes of operation using Transmit and Receive Processor data path configurations for system debug purposes.

A 16-bit generic register interface for access and configuration of internal memory mapped locations is included.

## FEATURES

- Suitable for FPGA and/or ASIC implementations.
- Integration support and maintenance available.
- XCS768F core available under flexible single use licensing terms with netlist or source code deliverables.
- Provides for bypass and normal (transport overhead processing) modes of operation.
- Implements 16-bit register interface for programming of internal registers.
- Compliant with ITU-T G.707 and Telcordia GR-253-CORE Specifications.
- Inserts transport overhead through internal register programming and/or external overhead ports.
- Provides transmit facility and terminal loopback options for diagnostic purposes.
- Supports auto generated or synchronized frame start generation.
- Supports transport overhead insertion and extraction through dedicated external section DCC, line DCC, section orderwire, line orderwire, and transport overhead ports.
- XCS768F Transmitter allows for blanking of all transport overhead locations except H1/H2/H3 bytes.
- Supports optional SONET/SDH frame scrambling/descrambling with programmable corruption capability for diagnostic purposes.
- Provides automatic REI insertion for B2 parity errors detected in the XCS768F Receive Processor.
- Allows for the insertion of programmable 1, 16 or 64 byte trace messages.
- Calculates and inserts B1/B2 parity information with optional corruption capability.
- Provides programmable internal registers for the insertion of selected transport overhead byte locations.
- Includes optional masking capability for all interrupt condition reporting.
- Allows for programmable automatic insertion of line RDI for the detection (XCS768F Receive Processor) of various error conditions.
- Supports programmable insertion of line AIS.
- Provides extended programmable diagnostics capability to force line AIS, LOS, RDI, and frame corruption insertion.
- Provides flexible frame alignment capability with programmable options for OOF and LOF algorithm state transitions. Diagnostic capability is provided to force LOF and OOF state conditions.
- Provides independent saturating performance counters (configurable for bit or block type) for the accumulation of OOF, B1, and REI errors with programmable latch and clear or incoming error sync capture options. Supports optional interrupt generation for OOF, B1, and REI error detection.
- Provides a 32-bit saturating performance counter (configurable for bit or block type) for the accumulation of B2 errors with programmable threshold capability (including optional error sync update capability). Provides optional interrupt generation for signal degrade (SD) and signal fail (SF) detection.

- Provides section trace interpreter with programmable trace accept and unstable counts for message lengths of 1, 16 or 64 bytes.
- Provides LOS detection through a selectable dedicated external input or programmable internal LOS state machine.
- Interprets and extracts F1, APS, S1 (optional byte or nibble detection) overhead information to internal register locations with programmable accept and inconsistent maskable interrupt capability.

**APPLICATIONS**

- OTN/SONET add/drop multiplexers
- SONET/SDH switch
- Digital cross connects
- OTN and/or SONET/SDH line cards
- Test equipment

**SONET/SDH Channelized Switch Application**

The SONET/SDH channelized switch application shown below is used to route channel payload data to/from various locations in a system. A series of line cards are plugged into a telecom bus backplane where channel information is routed through the use of a Channel Switch. The OC-768 line card contains cores for SONET/SDH Transport Processing (XCS768F) and channelized (STS-1 level) Pointer Processing (XCS768PP) providing full duplex capability at a data rate of 39.813Gb/s.

